

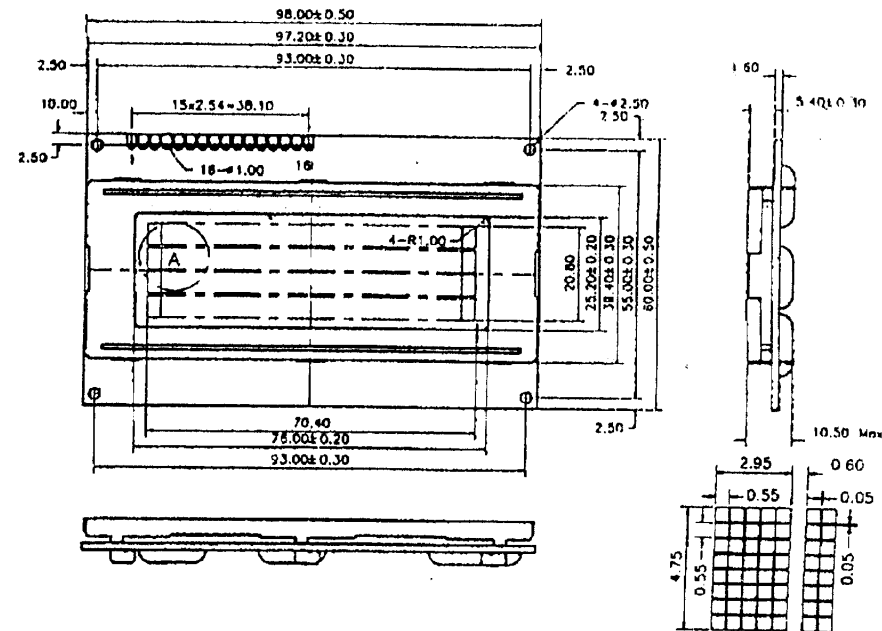
# Anschlußbelegung

Pin Nr.	Symbol	Wert	Funktion	
1	$V_{SS}$	-	0 V	Spannungsversorgung
2	$V_{DD}$	-	5 V	
3	$V_{EE}$	-	-	
4	RS	H/L	H:	Dateneingabe
			L:	Befehlseingabe
5	R/W	H/L	H:	Daten lesen
			L:	Daten schreiben
6	E	$E.E > L$	Enable Signal	
7	D0	H/L	Datenbus *	
8	D1	H/L		
9	D2	H/L		
10	D3	H/L		
11	D4	H/L		
12	D5	H/L		
13	D6	H/L		
14	D7	H/L		
15	A	-		
16	K	-		

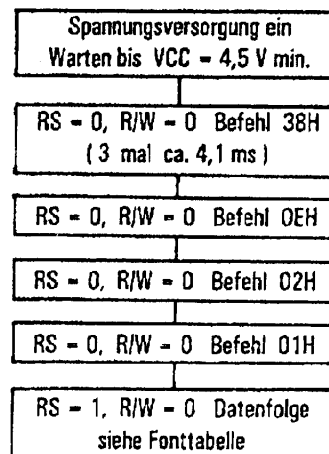
\* Bei 4-Bit Ansteuerung werden die 8-Bit (ASCII) Befehle / Daten geteilt. D.h. zuerst werden die höherwertigen 4 Bit und dann die niederwertigen 4 Bit über den 4-Bit Bus D4-D7 eingegeben. Die 8-Bit Ansteuerung erfolgt über den gesamten Bus D0-D7.

\*\* Anschluß LED-Version: Anode (+ 5 V), Kathode (0V)

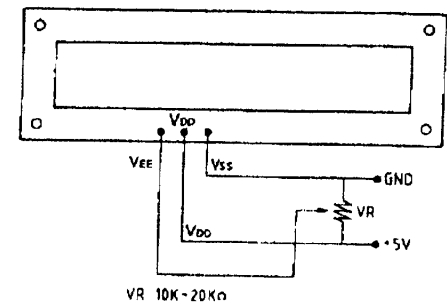
# DV-20400 20 Zeichen x 4 Zeilen Reflektiv / LED-Hinterleuchtung



## Testprogramm



## Anschlußplan: Spannungsversorgung



# INSTRUCTIONS

Instruction	Code										Description	Execution time (when fosc is 250 KHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear display	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (Address 0).	82 $\mu$ s ~ 1.04 ms
Return home	0	0	0	0	0	0	0	0	1	-	Returns the cursor to the home position (Address 0). Also returns the display being shifted to the original position. DD RAM contents remain unchanged.	40 $\mu$ s ~ 1.5 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies if or not to shift the display. These operations are performed during data write and read.	40 $\mu$ s
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of all display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40 $\mu$ s
Cursor and display shift	0	0	0	0	0	1	S/C	R/L	-	-	Moves the cursor and shifts the display without changing DD RAM contents	40 $\mu$ s
Function set	0	0	0	0	1	DL	N	F	-	-	Sets interface data length (DL) number of display lines (L) and character font (F).	40 $\mu$ s
Set CG RAM address.	0	0	0	1	A <sub>CG</sub>					Sets the CG RAM address. CG RAM data is sent and received after this setting.	40 $\mu$ s	
Set DD RAM address	0	0	1	A <sub>DD</sub>					Sets the DD RAM address. DD RAM data is sent and received after this setting.	40 $\mu$ s		
Read busy flag & address	0	1	BF	AC					Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	40 $\mu$ s		
Write data to CG or DD RAM	1	0	Write Data					Writes data into DD RAM or CG RAM.	40 $\mu$ s			
Read data to CG or DD RAM	1	1	Read Data					Reads data from DD RAM or CG RAM.	40 $\mu$ s			
I/D = 1: Increment I/D = 0: Decrement S = 1: Accompanies display shift. S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right. S/C = 0: Cursor move R/L = 0: Shift to the left. DL = 1: 8 bits DL = 0: 4 bits N = 1: 2 lines N = 0: 1 line F = 1: 5 x 10 dots F = 0: 5 x 7 dots BF = 1: Internally operating BF = 0: Can accept instruction											DD RAM: Display data RAM CG RAM: Character generator RAM A <sub>CG</sub> : CG RAM address A <sub>DD</sub> : DD RAM address Corresponds to cursor address. AC: Address counter used for both DD and CG RAM address.	Execution time changes when frequency changes. (Example) When fosc is 270 KHz: 40 $\mu$ s $\times$ $\frac{250}{270}$ = 37 $\mu$ s

UPPER 4 BIT HEXADECIMAL

		0	2	3	4	5	6	7	A	B	C	D	E	F
	Higher 4 bit Lower 4 bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
0	0000	CG RAM (1)	0001	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110
1	0001	(2)	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
2	0010	(3)	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111	
3	0011	(4)	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111		
4	0100	(5)	0101	0110	0111	1010	1011	1100	1101	1110	1111			
5	0101	(6)	0110	0111	1010	1011	1100	1101	1110	1111				
6	0110	(7)	0111	1010	1011	1100	1101	1110	1111					
7	0111	(8)	1010	1011	1100	1101	1110	1111						
8	1000	(9)	1011	1100	1101	1110	1111							
9	1001	(2)	1100	1101	1110	1111								
A	1010	(3)	1101	1110	1111									
B	1011	(4)	1110	1111										
C	1100	(5)	1111											
D	1101	(6)												
E	1110	(7)												
F	1111	(8)												

LOWER 4 BIT HEXADECIMAL